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A8. Abstract

The present invention relates to a circuit arrangement having
a load transistor (T1) and a current sensing transistor (T2)
5 coupled to the load transistor (T1), wherein a switch
arrangement (S) having at least one first switch (S1; S1a,
S1b) is connected downstream of the current sensing transistor
(T2) in order to connect the current sensing transistor (T2)
to a first or second evaluation circuit (BL1, BL2) depending
10 on a control signal.

A Figure 2

List of reference symbols

	Vdd	Supply potential
	IN	Input terminal
5	D	Drain terminal
	G	Gate terminal
	S	Source terminal
A	UDS1, UDS2	Drain-source voltage
	Uref	Reference voltage
10	K1	Comparator
	P11, 21, P12	Terminal pins
	BD	Bonding wire
	Z _L	Load
	BL1, BL2	Evaluation circuits
15	IC1, IC2	Integrated circuits
	Us1	First current signal
	Rs	Current sensing resistor
	K2	Comparator
	T2	Transistor
20	S1a, S1b	Transistors
	R1, R2	Resistors
	T4	Resistor
	Us2	Second current signal